What is claimed is:

1. An AGC amplifier circuit comprising:

a fixed-gain amplifier circuit whose gain is not controlled by an AGC voltage; and

a variable-gain amplifier circuit whose gain is controlled by the AGC voltage;

wherein, when the AGC voltage is within a predetermined voltage range, an overall gain of the AGC amplifier circuit is varied by the variable-gain amplifier circuit and, when the AGC voltage is outside the predetermined voltage range, the overall gain is kept constant by the fixed-gain amplifier circuit.

2. An AGC amplifier circuit as claimed in claim 1,

wherein a minimum gain of the AGC amplifier circuit is set to be equal to the gain of the fixed-gain amplifier circuit.

3. An AGC amplifier circuit comprising:

a fixed-gain amplifier circuit whose gain is not controlled by an AGC voltage;

a variable-gain amplifier circuit whose gain is controlled by the AGC voltage; and

input means for feeding an identical signal to the fixed-gain amplifier circuit and to the variable-gain amplifier circuit,

wherein, when an output of the variable-gain amplifier circuit exceeds an output of the fixed-gain amplifier circuit, the output of the fixed-gain amplifier circuit is delivered to an output terminal instead of the output of the variable-gain amplifier circuit, which is delivered to the output terminal otherwise.

4. An AGC amplifier circuit as claimed in claim 3,

wherein the fixed-gain amplifier circuit and the variable-gain amplifier circuit are each composed of a first differential amplifier circuit and a second differential amplifier circuit that are so connected as to share a common load resistor, and, in the second differential amplifier circuit constituting the variable-gain amplifier circuit, when a transistor to which the AGC voltage is applied and that is connected to the load resistor is brought into a cut-off state by the AGC voltage, only a current output from the first differential amplifier circuit constituting the fixed-gain amplifier circuit flows through the load resistor and a voltage appearing across the load resistor is delivered as the output of the fixed-gain amplifier circuit to the output terminal.

5. A satellite broadcast receiver apparatus comprising a first variable-gain amplifier circuit for amplifying a received radio-frequency signal, a mixer for performing frequency conversion to convert the amplified radio-frequency signal to an intermediate-frequency or baseband signal, a second variable-gain amplifier circuit for amplifying an output of the mixer, and an AGC voltage control circuit for feeding an AGC voltage first to the second variable-gain amplifier circuit and then to the first variable-gain amplifier circuit with a delay,

wherein the second variable-gain amplifier circuit comprises a fixed-gain amplifier circuit whose gain is not controlled by the AGC voltage, a variable-gain amplifier circuit whose gain is controlled by the AGC voltage, and input means for feeding an identical signal to the fixed-gain amplifier circuit and to the variable-gain amplifier circuit, wherein, when an output of the variable-gain amplifier circuit exceeds an output of the fixed-gain amplifier circuit, the output of the fixed-gain amplifier circuit is delivered to an output terminal instead of the output of the variable-gain amplifier circuit, which is delivered to the output terminal

otherwise

6. A satellite broadcast receiver apparatus as claimed in claim 5,

wherein the fixed-gain amplifier circuit and the variable-gain amplifier circuit are each composed of a first differential amplifier circuit and a second differential amplifier circuit that are so connected as to share a common load resistor, and, in the second differential amplifier circuit constituting the variable-gain amplifier circuit, when a transistor to which the AGC voltage is applied and that is connected to the load resistor is brought into a cut-off state by the AGC voltage, only a current output from the first differential amplifier circuit constituting the fixed-gain amplifier circuit flows through the load resistor and a voltage appearing across the load resistor is delivered as the output of the fixed-gain amplifier circuit to the output terminal.